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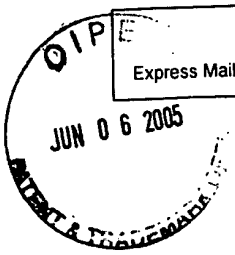

Express Mail Label No. Dated: _____

Docket No.: 08211/0200249-US0
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of:
Karthik R. Neravetla et al.

Patent No.: 6,861,881 B1

Issued: March 1, 2005

Certificate
JUN 1 3 2005
of Correction

For: FRACTIONAL CLOCK DIVIDER USING DIGITAL TECHNIQUES

REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 CFR 1.322 AND 37 CFR 1.323

MS Post Issue
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted an error which should be corrected.

The following errors were not in the application as filed by applicant:

In the Specification:

Column 5, Line 19, Delete "ncount_d=refhln 1" and insert - - ncount_d=refhln1 - -.

Column 9, Line 18 (Approx.) In Claim 15, insert -- a -- before "multiplexer".

The error was not in the application as filed by applicant; accordingly no fee is required.

Enclosed please find copies of pages 8 & 15.

JUN 1 3 2005

The following errors were found in the application as filed by applicant. The errors are now sought to be corrected are inadvertent typographical errors, the correction of which does not involve new matter or require reexamination.

Column 5, Line 41, After "same" insert --.--.

Transmitted herewith is a proposed Certificate of Correction effecting such amendment. Patentee respectfully solicits the granting of the requested Certificate of Correction.

Dated: June 6, 2005

Respectfully submitted,

By _____

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Application No. (if known): 10/674,874

Attorney Docket No.: 08211/0200249-US0

Certificate of Express Mailing Under 37 CFR 1.10

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Certificate of Correction (1 page)
Request for Certificate of Correction (2 pages)
Copies of Specification 8 & 15 (2 pages)
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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.	:	6,861,881 B1
APPLICATION NO.	:	10/674,874
ISSUE DATE	:	March 1, 2005
INVENTOR(S)	:	Karthik R. Neravetla et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specification:

Column 5, Line 19, Delete "ncount_d=refhln 1" and insert - - ncount_d=refhln1 - -.

Column 5, Line 41, After "same" insert --.--.

Column 9, Line 18 (Approx.) In Claim 15, insert -- a -- before "multiplexer".

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JUN 13 2005

ncount_d=refhln1. Alternatively, processing proceeds from decision block 420 to decision block 421 when either pcount_d≠refhlp1 or ncount_d≠refhln1. At block 430, signal CLK_D is adjusted such that signal CLK_D corresponds to a second logic level (e.g. low). Processing then proceeds from block 430 to block decision block 422. According to one example, decision blocks 420-422 are be performed simultaneously with combinational logic.

At decision block 421, a determination is made whether pcount_d=refhlp2 and ncount_d=refhlpn2. Processing proceeds from decision block 421 to block 430 when pcount_d=refhlp2 and ncount_d=refhln2. Alternatively, processing proceeds from decision block 421 to decision block 422 when either pcount_d≠refhlp2 or ncount_d≠refhln2. At decision block 422, a determination is made whether pcount_d=reflhp and ncount_d=reflhn. Processing proceeds from decision block 422 to decision block 424 when either pcount_d≠reflhp or ncount_d≠reflhn. Alternatively, processing proceeds from decision block 422 to block 432 when pcount_d=reflhp and ncount_d=reflhn. Although decision blocks 420-422 are illustrated as separate blocks, each of the comparisons may be performed at the same

At block 432, signal CLK_D is adjusted such that signal CLK_D corresponds to a first logic level (e.g. logic 1). Processing then proceeds from block 432 to block decision block 424. At decision block 424, a determination is made whether pcount_d has reached pmax (e.g. mul). Processing proceeds from decision block 424 to decision block 426 when pcount_d has not reached pmax. Alternatively, processing proceeds from decision block 424 to block 434 when pcount_d has reached pmax. At block 434, signal CLK_D is adjusted such that signal CLK_D corresponds to a first logic level (e.g. logic 1). Processing then proceeds from block 434 to block 436. At block 436, pcount_d is reset (e.g. to 1) at the next rising edge of signal CLK. Alternatively, pcount_d may be reset to 0 or some other value. Processing then proceeds from block 436 to decision block 426.

At decision block 426, a determination is made whether ncount_d has reached nmax (e.g. mul). Processing proceeds from decision block 426 to decision

asserted, and further configured to resume counting when a positive edge of the input clock signal occurs after the positive edge count enable signal is asserted, and wherein the second counter block is configured to reset the negative edge count value to zero and stop counting when the reset signal is asserted, and further configured to resume counting when a negative edge of the input clock signal occurs after the negative edge count enable signal is asserted.

15. The system of Claim 11, further comprising a jitter minimizing block comprising:

a first flip-flop that is configured to provide a first clock signal in response to the divided clock signal, wherein the first flip-flop is triggered on rising edges of the input clock signal;

a second flip-flop that is configured to provide a second clock signal in response to the divided clock signal, wherein the second flip-flop is triggered on falling edges of the input clock signal; and

a multiplexer that is configured to select the first clock signal as a jitter-minimized divided output clock signal when the input clock signal corresponds to a low logical level, and further configured to select the second clock signal as the jitter-minimized divided clock output signal when the input clock signal corresponds to a high logical level.

16. The system of Claim 11, wherein a first of the set of reference signals has an associated first reference value, a second of the set of reference signals has an associated second reference value, a third of the set of reference signals has an associated third reference value, a fourth of the set of reference signals has an associated fourth reference value, a fifth of the set of reference signals has an associated fifth reference value, a sixth of the set of reference signals has an associated sixth reference value, and wherein the decode logic block is arranged to provide the divided clock signal by: